S3C2450/16/51

400/533MHz

32-BIT CMOS

MICROCONTROLLER

Application Note

- Power Design Guide -

Revision 0.3

SAMSUNG ELECTRONICS

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Revision No	Description of Change	Refer to	Author(s)	Date
0.00	- Initial Release for review	-	K.Y.SHIM	June 30, 2008
0.30	- Revised Power on/off sequence	-	K.Y.SHIM	March 23, 2009

1. POWER DESIGN GUIDE

OVERVIEW

This document describes S3C2450/16/51 power design guide for circuit designer. It shows as follows,

- recommend DC operating conditions
- recommend system power design
- power on/off sequence
- PLL design guide
- power consumption data

It will help you design your system properly.

RECOMMENDED OPERATING CONDITIONS

Table 1-1. Recommended Operating Conditions (400MHz)

Parameter	Symbol		Min	Typ	Max	Unit
DC Supply Voltage for Alive Block	VDDalive		1.15	1.2	1.25	V
DC Supply Voltage for Core Block	ARMCLK / HCLK					
	400/133 MHz	VDDiarm VDDi VDDA_MPLL VDDA_EPLL	1.25	1.3	1.35	
DC Supply Voltage for I/O Block1	VDD_OP1**		1.7	1.8 / 2.5 /3.3	3.6	
DC Supply Voltage for I/O Block2	VDD_OP2		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for I/O Block3	VDD_OP3		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for USBOSC PAD	VDD_USBOSC		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for SRAM I/F	VDD_SRAM		1.7	1.8 / 2.5 /3.3	3.6	
DC Supply Voltage for SDRAM I/F	VDD_SDRAM		1.7	1.8 / 2.5	2.7	
DC Supply Voltage for RTC	VDD_RTC		1.7	1.8 / 2.5 / 3.0	3.3	
DC Supply Voltage for CAM/SD/LCD	VDD_CAM		1.7	1.8 / 2.5 / 3.3	3.6	
	VDD_SD		1.7	1.8 / 2.5 / 3.3	3.6	
	VDD_LCD		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for USB PHY 3.3V	VDDA33x		3.3-5%	3.3	3.3+5%	
DC Supply Voltage for USB PHY 1.2V	VDDI_UDEV		1.2-5%	1.2	1.2+5%	
DC Supply Voltage for ADC	VDDA_ADC		3.0	3.3	3.6	
DC Input Voltage	V_{IN}		3.0	3.3	3.6	
			2.3	2.5	2.7	
			1.7	1.8	1.95	
DC Output Voltage	V_{OUT}		3.0	3.3	3.6	
			2.3	2.5	2.7	
			1.7	1.8	1.95	
Operating Temperature	TA		Industrial	-40 to 85		°C
			Extended	-20 to 70		

NOTE 1: **If not use USB function, VDD_OP1 have a range from 2.3V to 3.6V.

NOTE 2: S3C2416X does not support VDD_CAM conditions.

Table 1-2. Recommended Operating Conditions (533MHz)

Parameter	Symbol		Min	Typ	Max	Unit
DC Supply Voltage for Alive Block	VDDalive		1.15	1.2	1.25	V
DC Supply Voltage for Core Block	ARMCLK / HCLK					
	533/133 MHz	VDDiarm	1.275	1.325	1.375	
		VDDi VDDA_MPLL VDDA_EPLL	1.15	1.2	1.25	
DC Supply Voltage for I/O Block1	VDD_OP1**		1.7	1.8 / 2.5 /3.3	3.6	
DC Supply Voltage for I/O Block2	VDD_OP2		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for I/O Block3	VDD_OP3		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for USB OSC PAD	VDD_USBOSC		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for SRAM I/F	VDD_SRAM		1.7	1.8 / 2.5 /3.3	3.6	
DC Supply Voltage for SDRAM I/F	VDD_SDRAM		1.7	1.8 / 2.5	2.7	
DC Supply Voltage for RTC	VDD_RTC		1.7	1.8 / 2.5 / 3.0	3.3	
DC Supply Voltage for CAM/SD/LCD	VDD_CAM		1.7	1.8 / 2.5 / 3.3	3.6	
	VDD_SD		1.7	1.8 / 2.5 / 3.3	3.6	
	VDD_LCD		1.7	1.8 / 2.5 / 3.3	3.6	
DC Supply Voltage for USB PHY 3.3V	VDDA33x		3.3-5%	3.3	3.3+5%	
DC Supply Voltage for USB PHY 1.2V	VDDI_UDEV		1.2-5%	1.2	1.2+5%	
DC Supply Voltage for ADC	VDDA_ADC		3.0	3.3	3.6	
DC Input Voltage	V_{IN}		3.0	3.3	3.6	
			2.3	2.5	2.7	
			1.7	1.8	1.95	
DC Output Voltage	V_{OUT}		3.0	3.3	3.6	
			2.3	2.5	2.7	
			1.7	1.8	1.95	
Operating Temperature	TA		Industrial	-40 to 85		°C
			Extended	-20 to 70		

NOTE 3: **If not use USB function, VDD_OP1 have a range from 2.3V to 3.6V.

NOTE 4: S3C2416X does not support 533MHz conditions.

RECOMMEND SYSTEM POWER DESIGN

(1) Power generation using controllable PMIC

Recommended Power on sequence: Alive -> Core -> I/O with Memory -> nRESET

When All of Power source must be controlled by PMIC, PWREN is no meaningful when power on/off reset.
In order to enter/exit the SLEEP mode, PWREN signal is used for controlling on/off core power. System designer has to make this manner.

(2) Power generation using Discrete Buck & LDO Regulator

Recommended Power on sequence: I/O with Memory -> Alive -> Core(controlled by PWREN) -> nRESET

PWREN signal is invoked when I/O power is on & waked up from SLEEP mode. So it is easy to make this PWREN signal to use core power enable signal as these two cases. In this case, we recommend this power on sequence. System designer easily makes its system as this manner.

Note) Alive part I/O signal has unknown state which is described in the Figure 1-3. Power on sequence.
At this time, Some I/O signal may occur glitch, but has no problem to enter the normal operation mode. For example, when using this I/O as LED on/off control signal, it causes unwanted flickering.
To protect this glitch, System designer can use external AND gate device with nRESET signal.

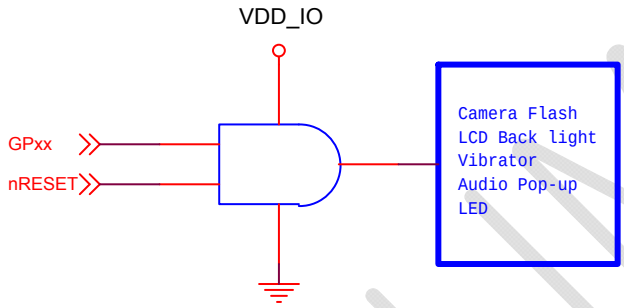

Table 1-3. 400MHz operating voltage

Power Pins	Voltage spec.	Normal operating voltage
VDDiarm VDDi/VDDmpll/VDDepll	1.25V ~ 1.35V	1.3V

Table 1-4. 533MHz operating voltage

Power Pins	Voltage spec.	Normal operating voltage
VDDarm	1.275V ~ 1.375V	1.325V
VDDi/VDDmpll/VDDepll	1.15V ~ 1.25V	1.2V

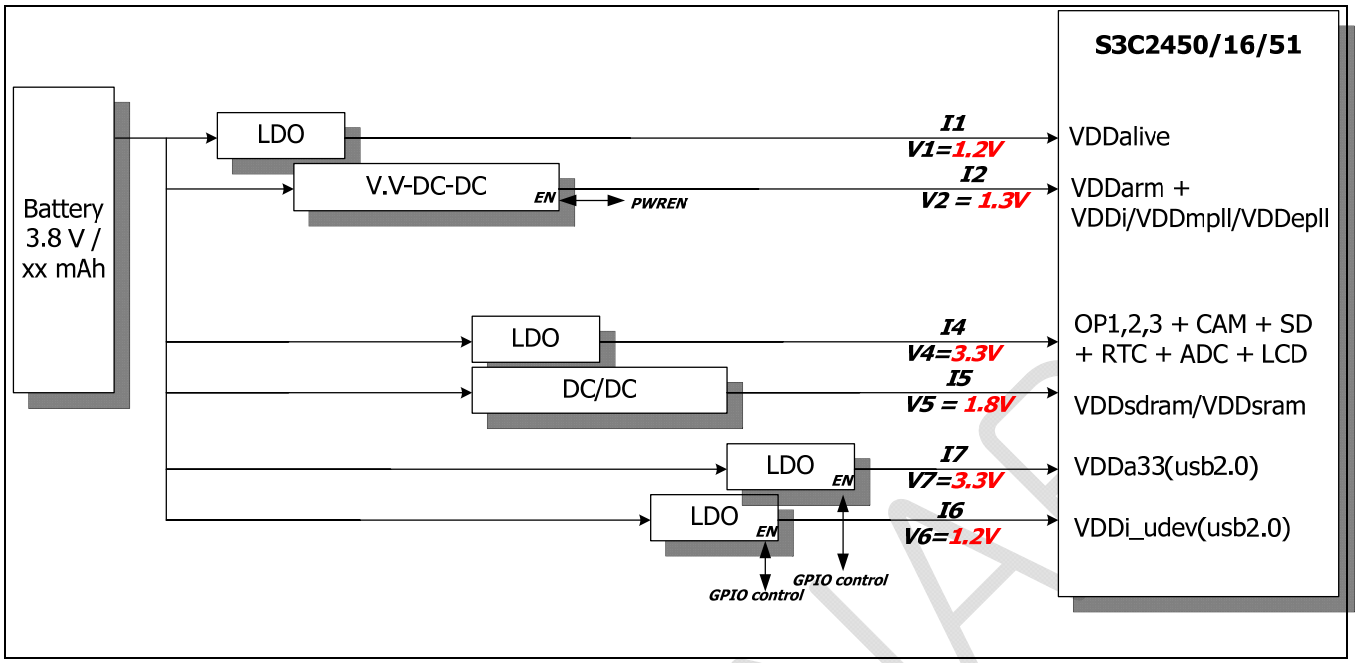

Figure 1-1. Power Scheme Diagram: (400MHz)

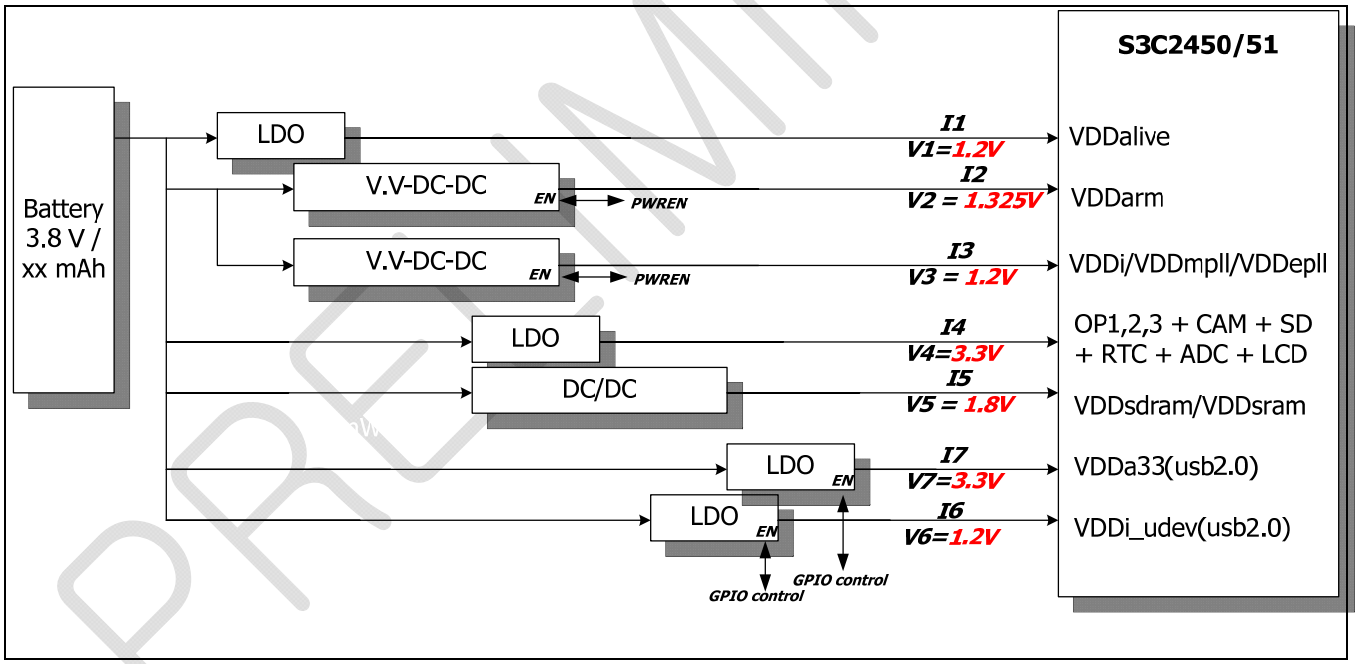

Figure 1-2. Power Scheme Diagram : (533MHz)

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POWER ON and OFF SEQUENCE

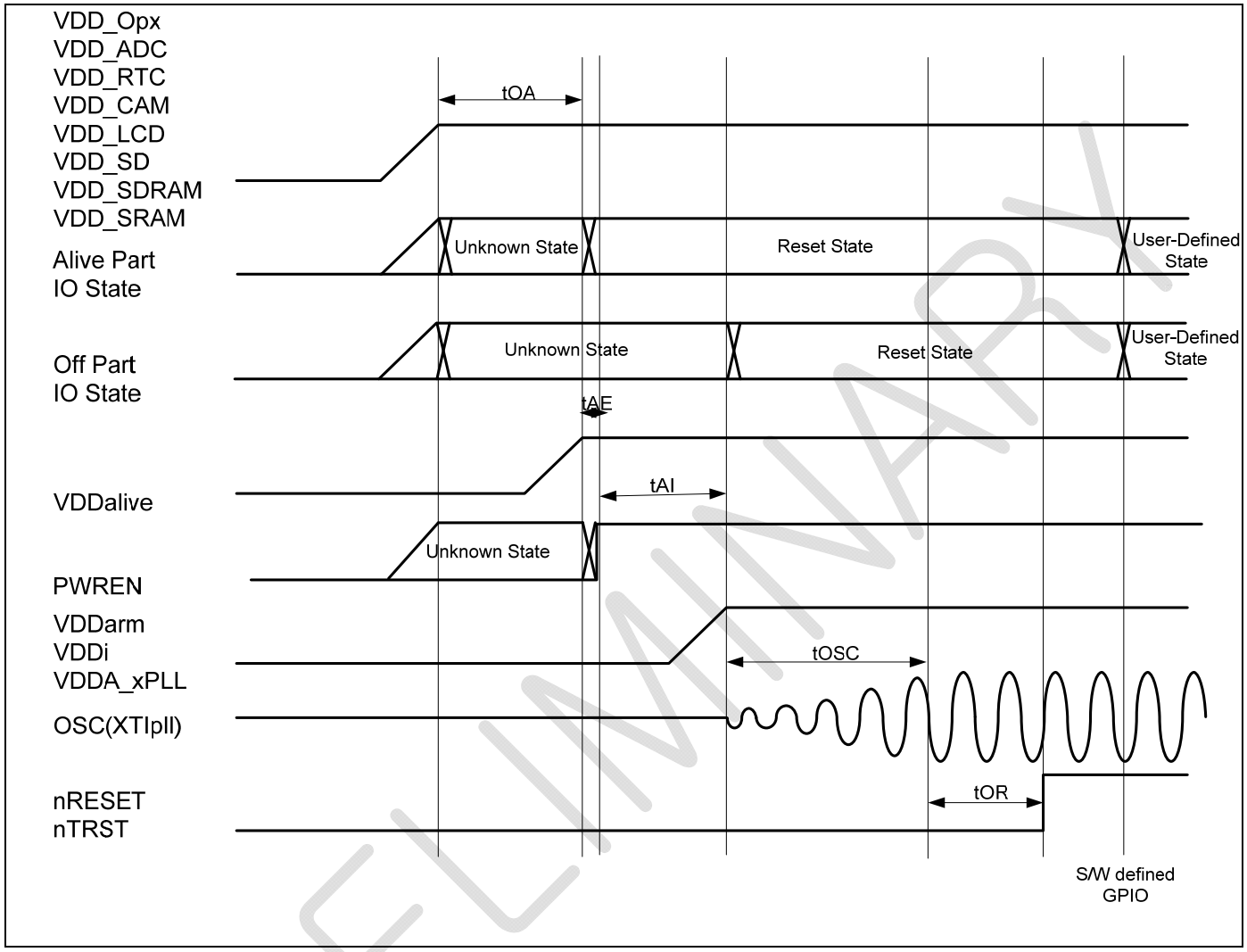
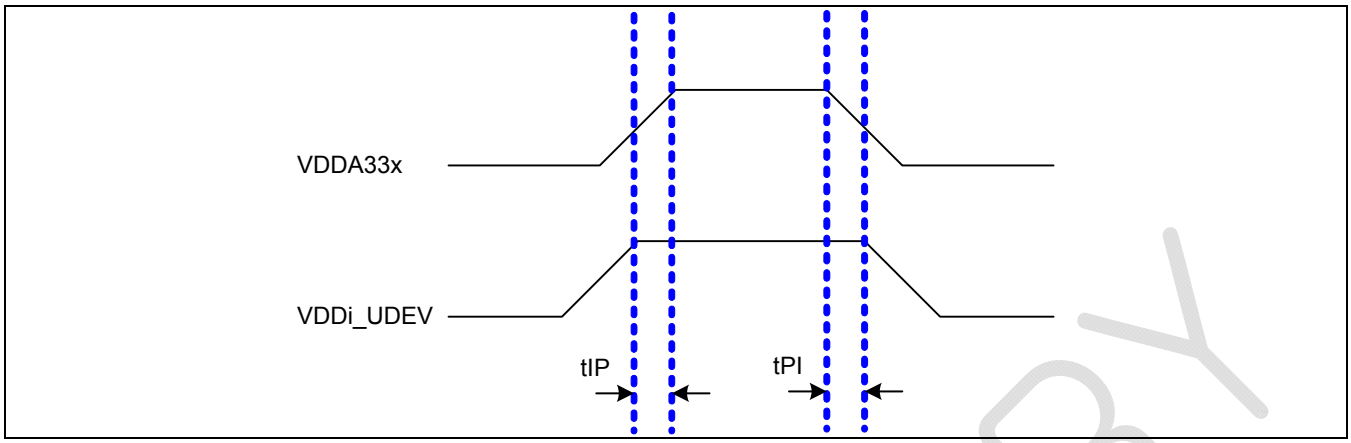


Figure 1-3. Power on sequence

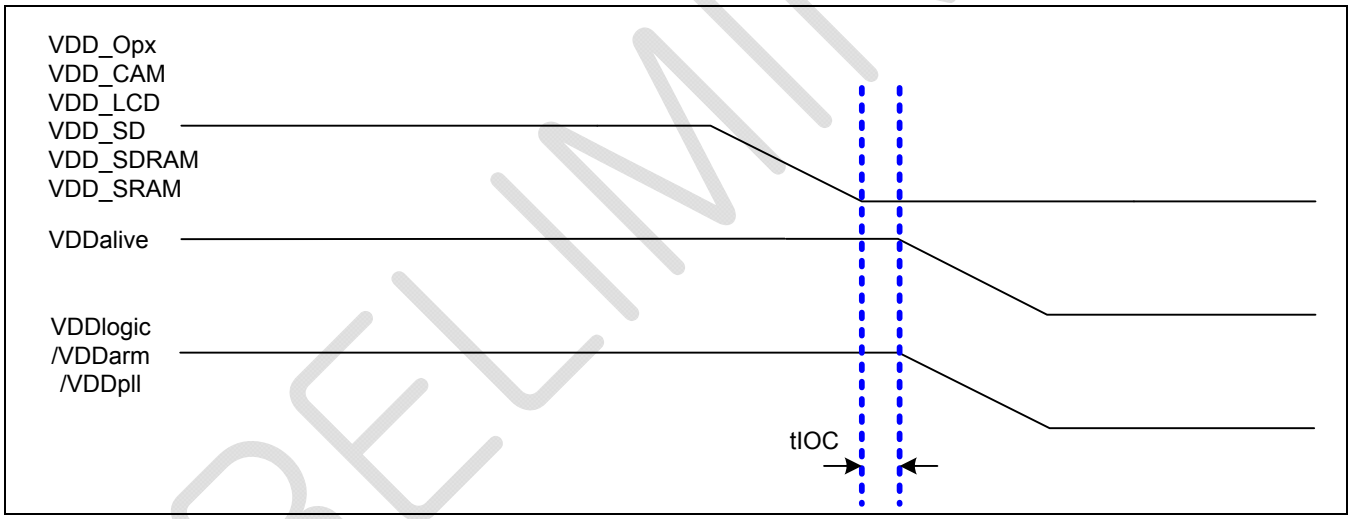
Table 1.5 Power on Reset Timing Specifications

Symbol	Description	Min	Typical	Max	Units
tOA	VDDpadIO to VDDalive	0			ms
tAI	VDDalive to VDDarm/i/xpll	It depends on Regulator.			us
tAE	VDDalive to PWREN	0		10	ns
tOSC	VDDarm/i/xpll to Oscillator stabilization		500		us
tOR	Oscillator stabilization to nRESET & nTRST high	10			cycle



Symbol	Description	Min	Typical	Max	Units
tIP	VDDi_UDEV to VDDA33x	0			ms
tPI	VDDA33x to VDDi_UDEV	0			ms

Figure 1-4. USB power on/off sequence



Symbol	Description	Min	Typical	Max	Units
tIOC	VDDpadIO to VDDcore(VDDalive/VDDiarm/VDDi/VDDpll)	0			ms

Figure 1-5. Power off sequence

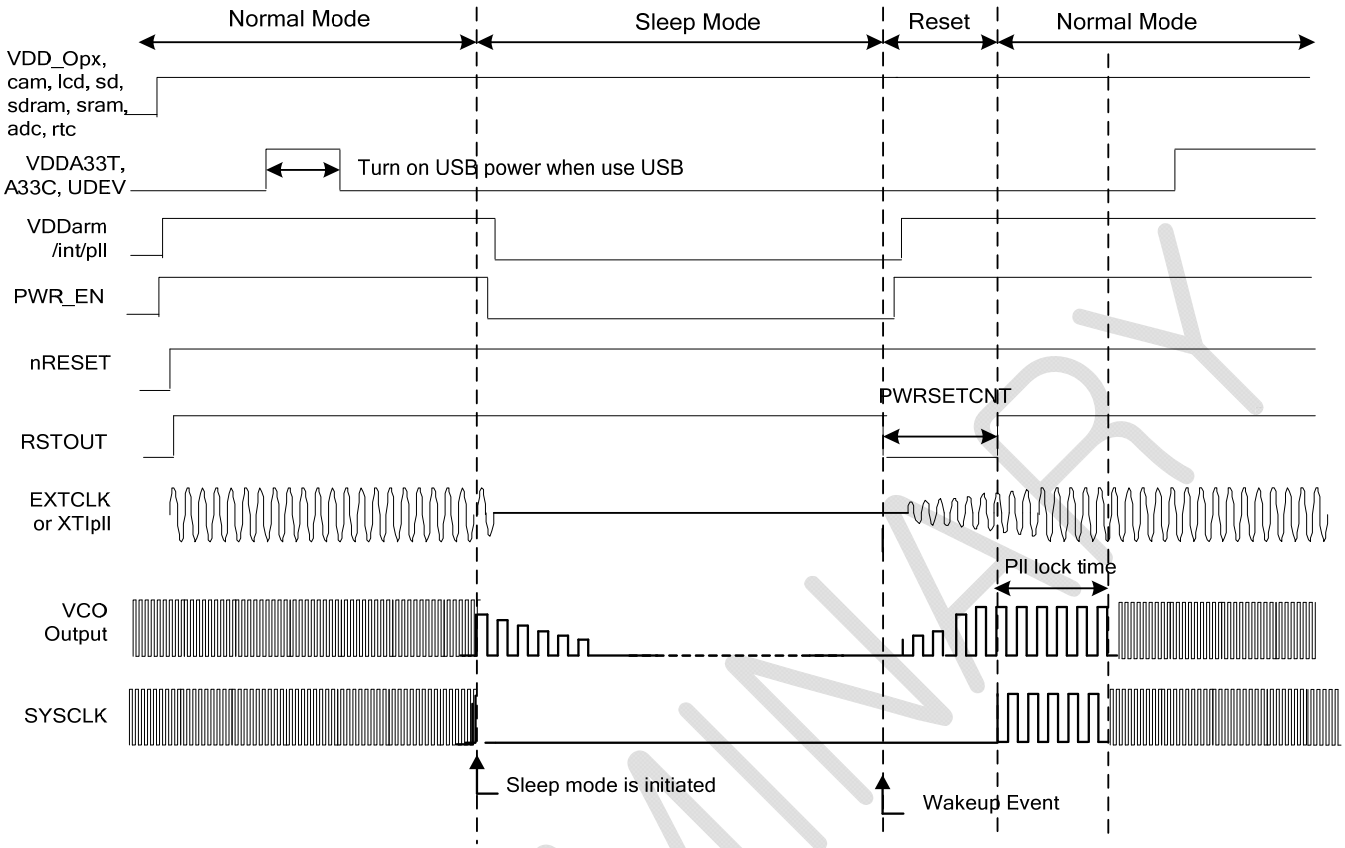


Figure 1-6. Sleep mode & wakeup sequence

PLL DESIGN GUIDE

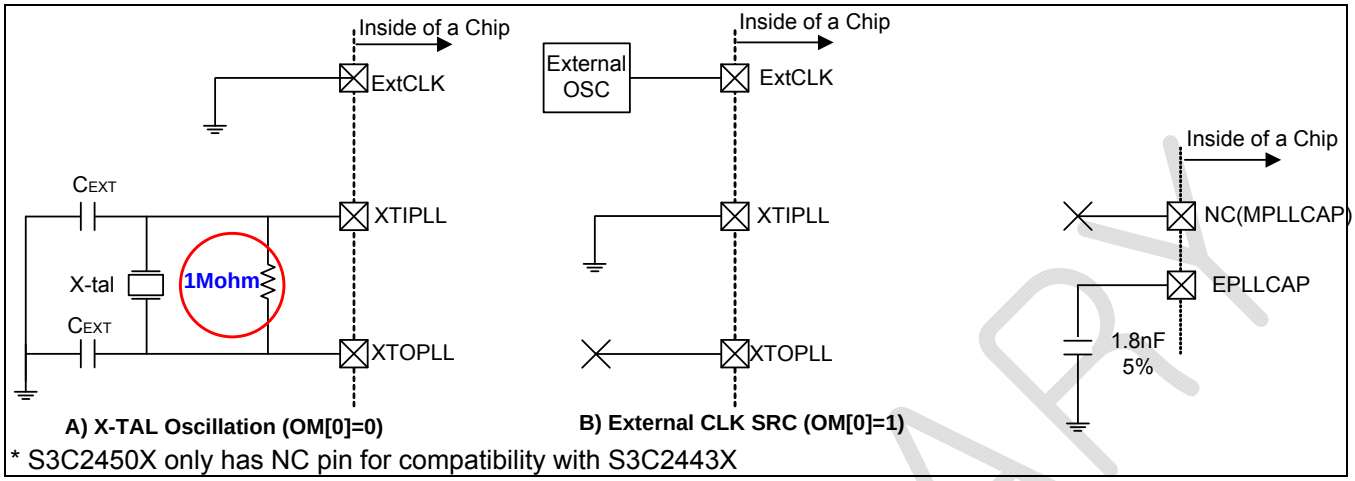


Figure 1-7. Main Oscillator circuit examples

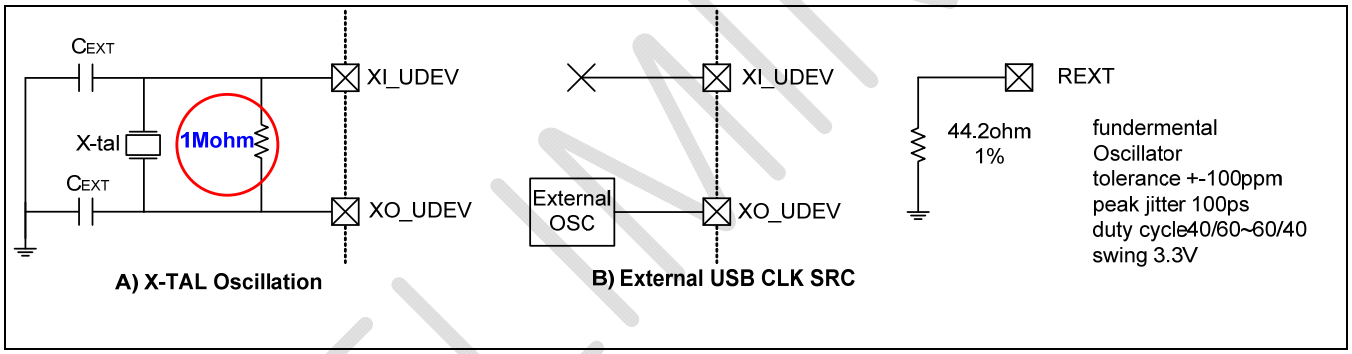


Figure 1-8. USB Oscillator circuit examples

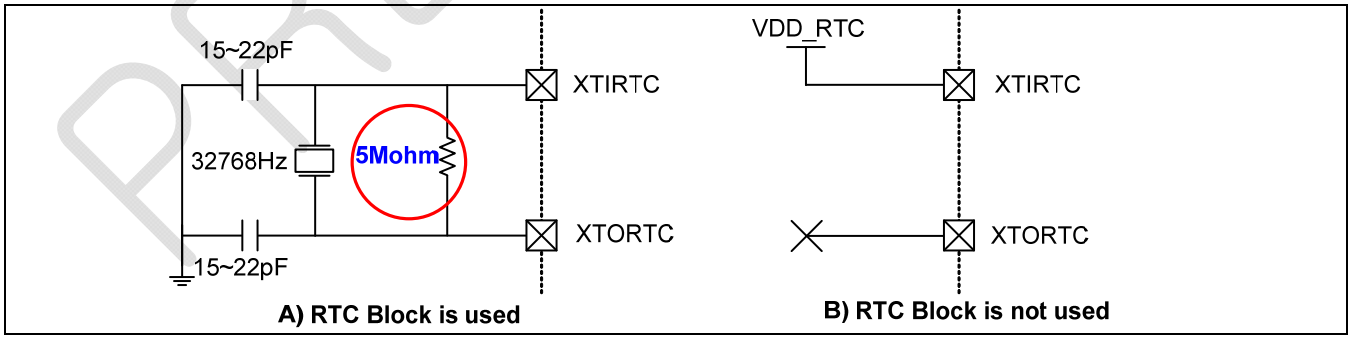


Figure 1-9. RTC Oscillator circuit examples

(1) MPLL Specification

The output frequencies of **MPLL** can be calculated using the following equations:

$F_{OUT} = (m \times F_{IN}) / (p \times 2^{S})$ (should be 40~1600MHz)

$Fvco = (m \times F_{IN}) / p$ (should be 800~1600MHz)

where, m = MDIV, p = PDIV, s = SDIV, Fin = 10~30Mhz

Don't set the value PDIV[5:0] or MDIV[9:0] to all zeros. (6'b00 0000 / 10'b00 0000 0000)

NOTE: Although there is the equation for choosing PLL value, we strongly recommend only the values in the PLL value recommendation table. If you have to use other values, please contact us.

FIN (MHz)	Target FOUT (MHz)	MDIV (decimal)	PDIV (decimal)	SDIV (decimal)	Duty
12	240	320	4	2	40~60%
12	400	400	3	2	40~60%
12	450	225	3	1	40~60%
12	500	250	3	1	40~60%
12	533	267	3	1	40~60%
12	600	300	3	1	40~60%
12	800	400	3	1	40~60%

(2) EPLL Specification

The output frequencies of **EPLL** can be calculated using the following equations:

$F_{OUT} = ((m+k/2^{16}) \times FIN) / (p \times 2^{S})$ (should be 20~100MHz)

$Fvco = (m \times F_{IN}) / p$

where, m = MDIV, p = PDIV, s =SDIV, k = KDIV Fin = 10~40MHz

Don't set the value PDIV[5:0] or MDIV[7:0] to all zeros. (6'b00 0000 / 8'b0000 0000)

NOTE: Although there is the equation for choosing PLL value, we strongly recommend only the values in the PLL value recommendation table. If you have to use other values, please contact us.

FIN (MHz)	FOUT (MHz)	MDIV (decimal)	PDIV (decimal)	SDIV (decimal)	KDIV (decimal)	Error [%]
12	36	48	1	4	0	0
12	48	32	1	3	0	0
12	60	40	1	3	0	0
12	72	48	1	3	0	0
12	84	28	1	2	0	0
12	96	32	1	2	0	0

(3) Usual Conditions for MPLL/EPLL & Clock Generator

PLL & Clock Generator generally use the following conditions.

Table 1.6 MPLL/EPLL & Clock Generator condition

Loop filter capacitance	C_{LF}	MPLLCAP : N/A
		EPLLCAP :Typical 1.8nF 5%
Fin	-	MPLL: 10 – 30 MHz EPLL: 10 – 40 MHz
Fout	-	MPLL: 40 – 1600 MHz EPLL: 20 – 100 MHz
External capacitance used for X-tal	C_{EXT}	15 pF
Feedback Resistor used for X-tal	R_F	1M Ω

(4) USB2.0 PLL Specification

PLL & Clock Generator generally uses the following conditions.

Table 1.7 USBPLL & Clock Generator condition

REXT	R	44.2Ω ± 1%
VDDA33V	V	3.3V (± 5%)
VDDI_UDEV	V	1.2V (± 5%)
External X-tal frequency	-	12M/24M/48 MHzI Recommend a quartz crystal
External capacitance used for X-tal	C_{EXT}	12M/24MHz - 20 pF 48MHz - 16 pF

NOTE: For usb2.0 device, user should obey a layout rule of PCB.